AMENDMENTS TO THE CLAIMS

Please amend the present application as follows:

Claims

1. (Currently amended) A method for reducing variations in noise and temperature in a mixed-signal circuit, the method comprising:

providing a memory ~~electrically proximate an analog circuit~~ comprising a dummy memory and an acquisition memory;

receiving a digital data word at the memory;

~~determining whether the data word is a desired data word;~~

performing a write to the acquisition memory when the data is a *n*-th data word in a repeating set of *n* data words; and

performing a dummy write to the dummy memory when the data word is not ~~a desired~~ the *n*-th data word. ~~; and~~

~~writing the data word to the memory when the data word is a desired data word.~~

2. (Currently amended) The method of claim 1, ~~in which~~ further comprising:

~~the receiving comprises~~ processing an analog input signal to generate the *n*-th data word. ~~and generating the digital data words.~~

3. (Currently amended) The method of claim 1, in which:

the ~~memory comprises~~ dummy memory ~~and~~ is the same as the acquisition memory. ~~;~~

~~the performing comprises performing the dummy write to the dummy memory; and~~

~~the writing comprises writing the data word to the acquisition memory.~~

4. (Currently amended) The method of claim 1, ~~in which~~ further comprising:

~~the determining comprises:~~

providing an enable signal having a dummy value and an acquisition value; and ~~, and~~

~~determining whether the enable signal is at the dummy value or the acquisition value;~~

~~the performing comprises~~ performing the dummy write to the dummy memory when the enable signal is at the dummy value. ~~; and~~

~~the writing comprises writing the data word to the memory when the enable signal is at the acquisition value.~~

5. (Canceled)

6. (Currently amended) The method of claim ~~5~~1, in which the dummy memory comprises no more than a single memory location in the memory.

7. (Currently amended) The method of claim ~~5~~1, in which the dummy memory comprises a range of memory locations in the memory.

8-12. (Canceled)

13. (Currently amended) A mixed-signal circuit, comprising:

an analog circuit;

~~memory electrically proximate to the analog circuit, the memory connected to receive digital data words~~ a memory configured to receive data words; and

a memory controller ~~connected~~ coupled to the memory, the memory controller operable ~~to cause the memory~~ to write to the memory ~~each of the data words that is~~ every *n*-th data word in a stream of data words as a desired data word and additionally to perform a dummy write to memory for each of the other data words ~~that is not a desired data word.~~ in the stream of data words wherein each of the other data words comprises a dummy data word.

14. (Currently amended) The circuit of claim 13, additionally comprising an analog/digital circuit operable to process an analog input signal ~~and to generate~~ for generating the *n*-th data word. ~~digital data words.~~

15. (Currently amended) The circuit of claim 14, in which the analog/digital circuit comprises an analog-to-digital converter.

16. (Currently amended) The circuit of claim 13, in which:

the memory controller is responsive to an enable signal for generating ~~and generates~~ an address signal;

the enable signal has a dummy value when the data word is not ~~a desired~~ the *n*-th data word and an acquisition value when the data word is ~~a desired~~ the *n*-th data word;

the memory comprises dummy memory and acquisition memory~~, and stores the data~~

~~word where designated by the address signal~~; and

the memory controller provides ~~the~~ a first address signal corresponding to the dummy memory when the enable signal is at the dummy value and provides ~~the~~ a second address signal corresponding to the acquisition memory when the enable signal is at the acquisition value.

17. (Original) The circuit of claim 16, in which the dummy memory comprises a single memory location in the memory.

18. (Currently amended) The circuit of claim 16, in which the first address signal is the same as the second address signal. ~~dummy memory comprises a range of memory locations in the memory.~~

19. (Currently amended) ~~The circuit of claim 13, in which~~ A mixed-signal circuit, comprising:

an analog circuit;

~~the~~ a memory controller ~~is~~ responsive to a decimation ratio signal ~~and generates~~ for generating an address signal;

~~the circuit additionally comprises~~ a decimator operable in response to the decimation ratio signal to generate output data words ~~in response to the data words, the output data words~~ comprising, in a given number of clock cycles, ~~respective dummy data words~~ a dummy data word and a desired data word; and

~~the~~ a memory ~~is connected~~ operable to receive the output data words from the decimator and ~~stores the output data words~~ to store the dummy data word and the desired data word where designated by the address signal in each of the clock cycles. ~~; and~~

~~the memory controller is operable to maintain the address signal at one value during the given number of clock cycles.~~

20. (Original) The circuit of claim 19, in which the memory controller is operable to change the address signal after the last of the given number of clock cycles.

21. (Original) The circuit of claim 19, in which the memory controller includes the decimator.

22. (Currently amended) The circuit of claim 13, in which:

the memory controller generates an address signal;

the memory stores the dummy data word and the desired data word where designated by the address signal in each clock cycle; and

the memory controller is operable to maintain the address signal for ~~a given number~~ *n* number of clock cycles ~~and changes the address signal after the given number of clock cycles~~.

23. (New) The circuit of claim 22, in which:

the memory controller is operable to change the address signal after *n* number of clock cycles.

24. (New) The circuit of claim 13, in which:

the memory controller is operable to generate a first address signal for a *n*-th clock cycle in a set of *n* clock cycles and a second address signal for the other clock cycles; and

the memory stores the desired data word where designated by the first address signal and the each of the other data words where designated by the second address signal.

25. (New) The circuit of claim 24, in which the first address signal is the same as the second address signal.

26. (New) The method of claim 1, further comprising:

using a decimating ratio to generate the set of n data words whereby the n-th data word is a desired data word and the remaining data words in the set of n data words are dummy data words.